Holistic Lithography

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INVESTOR DAY
ASMLSMALLTALK2014
LONDON

Holistic Lithography – Introduction

Customer Problem:

- Beyond 20nm node scanner and non scanner contributions must be addressed to meet patterning performance requirements

ASML Holistic Lithography:

- ASML provides a unique and comprehensive holistic capability via integration of scanner with computational lithography, metrology sensors feeding into scanner knobs to control the process
- The scanner is the only manufacturing tool processing and controlling the wafer at field / die level

Customer benefits:

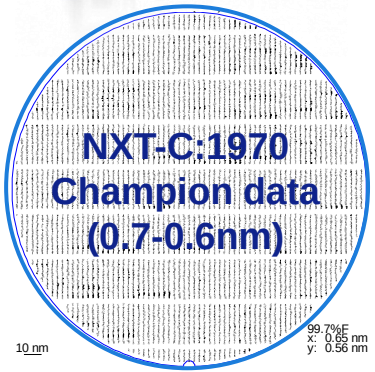
- Increased collaboration and technical intimacy with ASML experts & solutions enable faster and better ramp
- Yield is improved, rework & cycle time are reduced

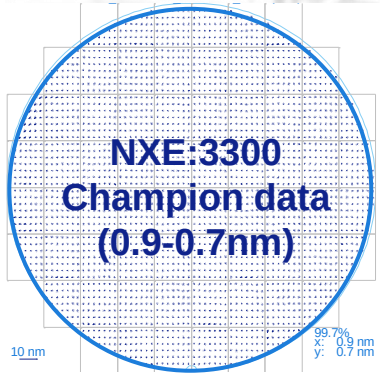
ASML business opportunity

- Holistic lithography revenue opportunity of 1B€ within next 3 years (>20% per year), at very good margins

Customer problem: scanner **and** non scanner contributors to patterning performance must be addressed – example Overlay

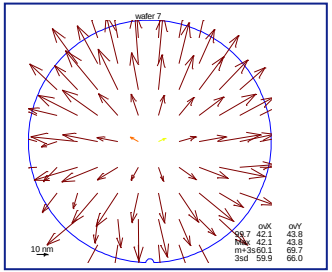
Scanner Overlay Error Contribution



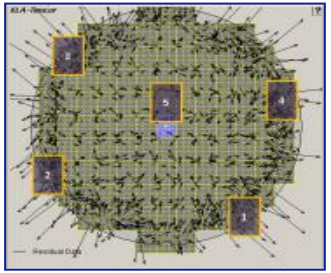


NXT-C:1970 & NXE:3300 - Scanner OVERLAY < 2nm

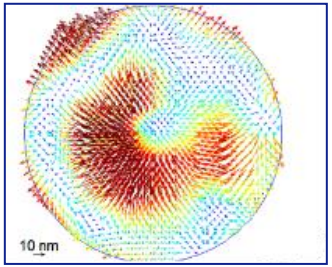
Other Overlay Error Contributors



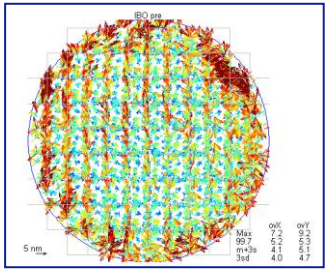
Wafer alignment



Etch fingerprint



CMP fingerprint



Metrology accuracy

On product OVERLAY > 6nm

ASML holistic lithography: links the scanner to YieldStar metrology and computational lithography design context

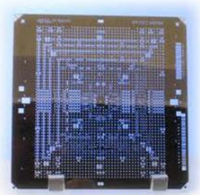
NXT - Immersion

NXE - EUV

1.Advanced lithography capability

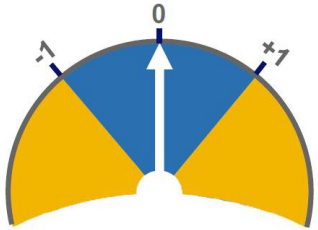
4. Process Window Enlargement

5. Process Window Control



Product reticles

3- Computational Lithography Design context

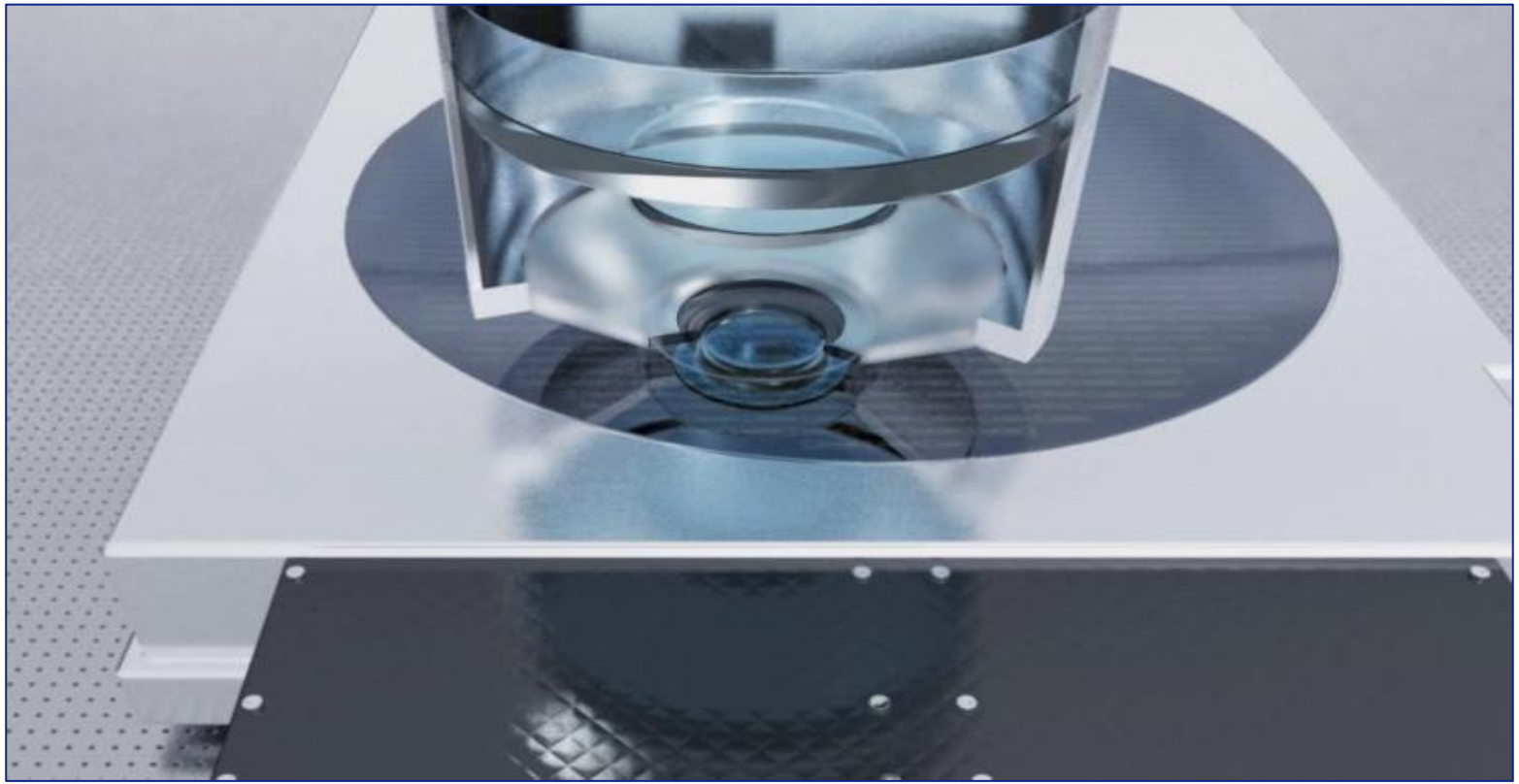


6. Process window detection

Product wafers

2- YieldStar Metrology and Control SW

Why ASML?: Scanner is the only tool processing and controlling the wafer at field level



Why ASML?: Multiple scanner knobs enable in-line optimization of patterning performance

Interfaces (knobs)

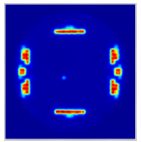
I — Illumination

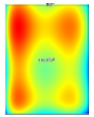
D — Dose

O — Overlay

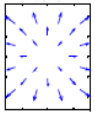
L — Lens

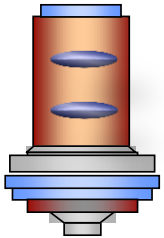
F — Focus

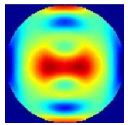




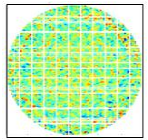
Reticle stage





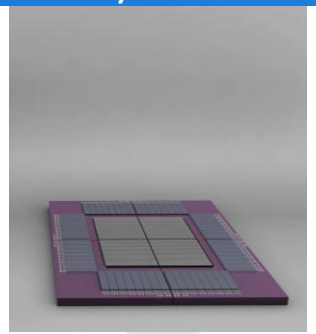


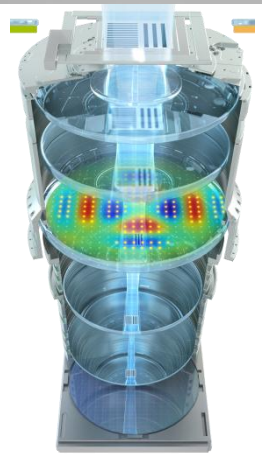
Wafer stage



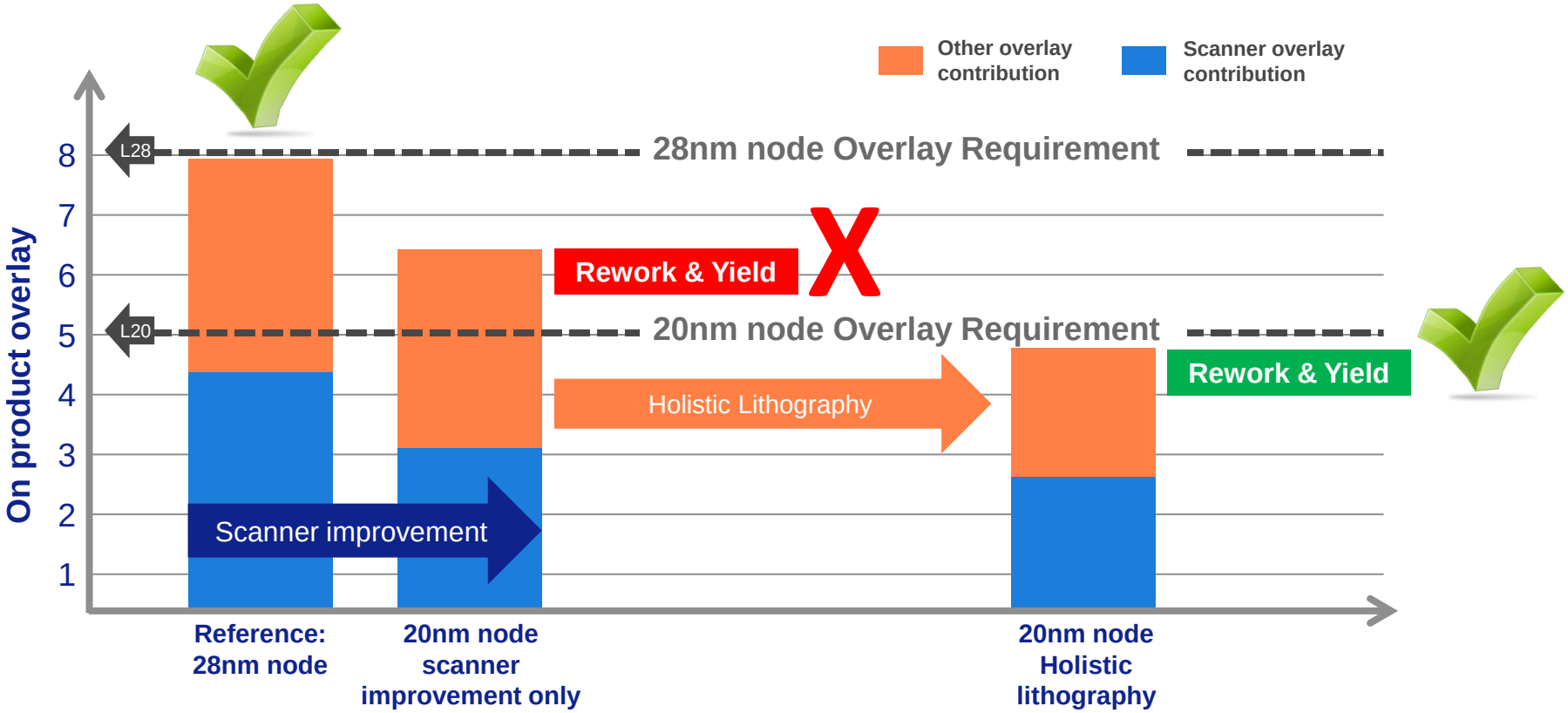
actuators

FlexRay illuminator

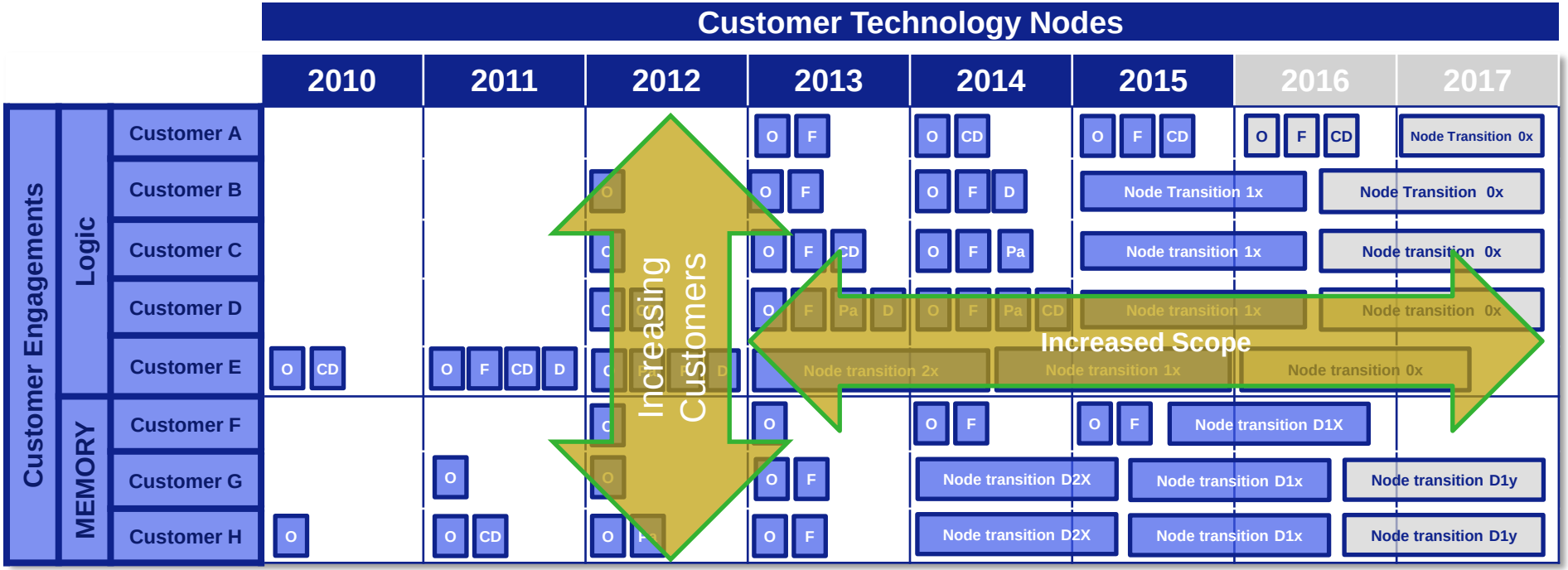




Customer benefits: Adoption of holistic lithography at 20nm node enables customers to meet patterning requirements



ASML is working intimately with its customers to deliver patterning requirement through our expert support



CD= Imaging (CDU) D= Defectivity F= Focus, O = Overlay, Pa = Patterning (Computational lithography), Node transition = multiple competencies for entire node

ASML will build and implement holistic lithography infrastructure over the next 5 years

1

2012	2013	2014	2015	2016	2017	2018	2019	2020

Ramp
Volume

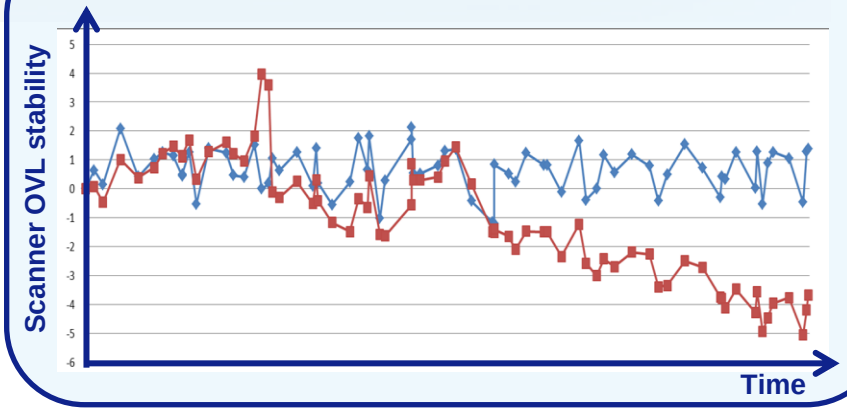
Standalone YieldStar

Test wafers

Overlay, Focus

(Low frequency, dense data)

Scanner stable +- 1nm over 12 months



Metrology
Control

ASML will build and implement holistic lithography infrastructure over the next 5 years

2

2012	2013	2014	2015	2016	2017	2018	2019	2020

Ramp
Volume

Standalone YieldStar

Integrated YieldStar

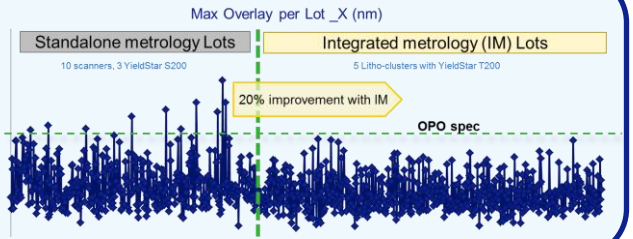
Test wafers

Overlay, Focus
(Low frequency, dense data)

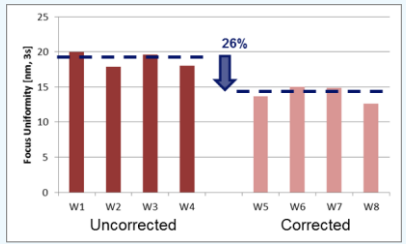
Product wafers

Overlay, Focus &CD after Lithography
(High frequency, sparse data)

20% overlay improvement



20% focus improvement



ASML will build and implement holistic lithography infrastructure over the next 5 years

Next | 2012 | 2013 | 2014 | 2015 | 2016 | 2017 | 2018 | 2019 | 2020

Ramp
Volume

Standalone YieldStar

Integrated YieldStar

Standalone YieldStar

ETCH

Test wafers

Overlay, Focus
(Low frequency, dense data)

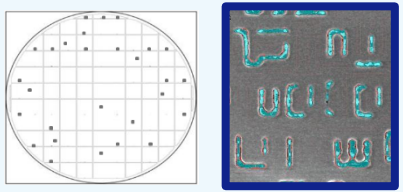
Product wafers

Overlay, Focus &CD after Lithography
(High frequency, sparse data)

CD After Etch
(High frequency, sparse data)

Off Tool Server
(LithoInsight)

Process window optimizer



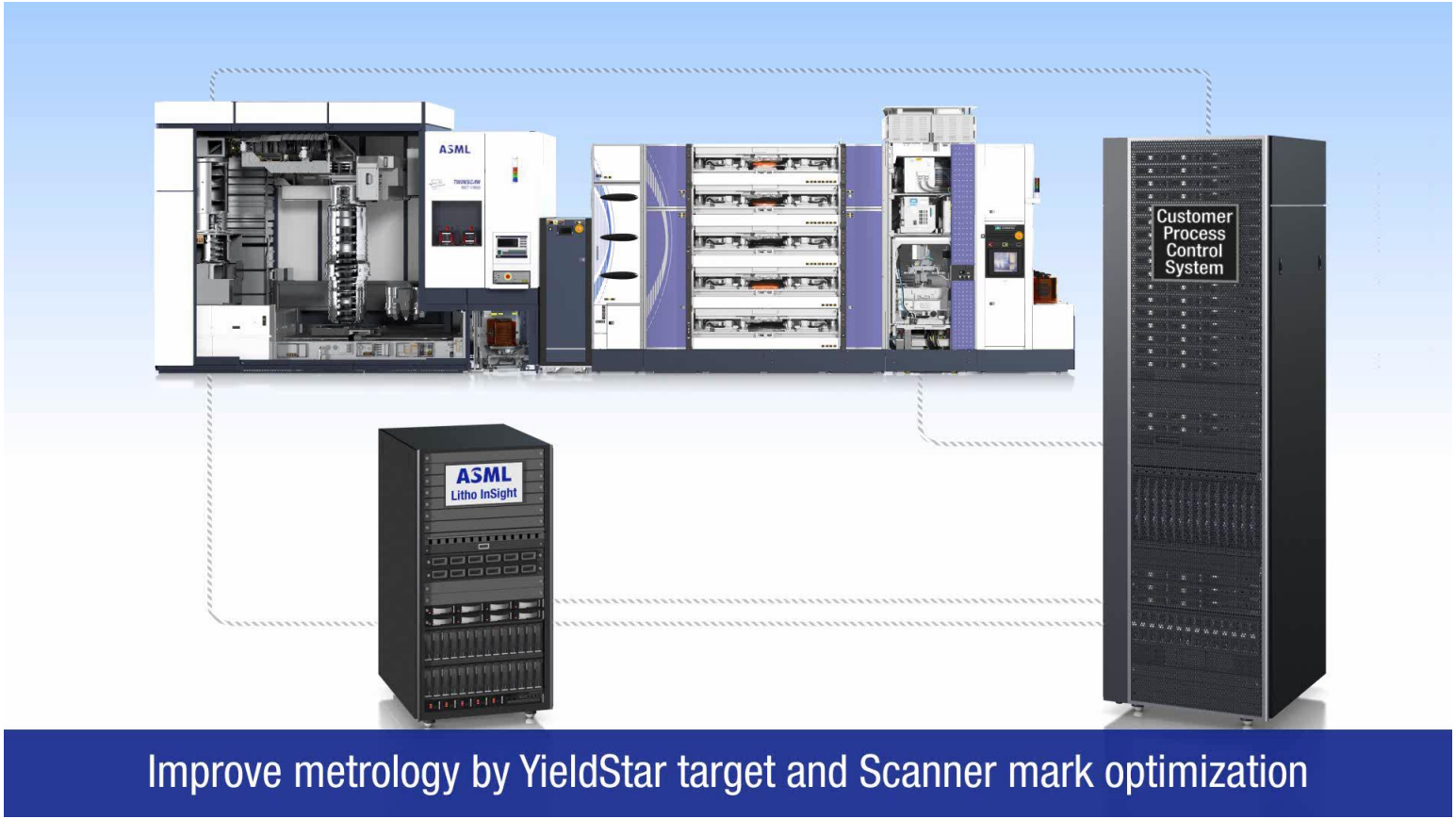
Metrology
Control

So far: BRION computational lithography continues to extend process window, also using scanners interfaces

ASML

ASML Holistic Lithography™
Full–chip Source and Mask Optimization

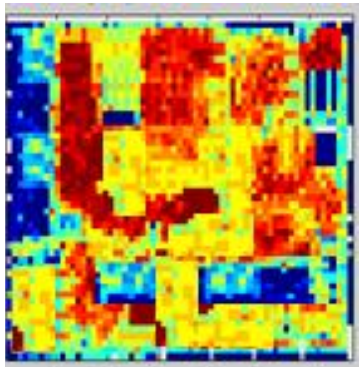
Now: Computational lithography enters wafer fab to provide design context to metrology…



… and control software – Process window optimization

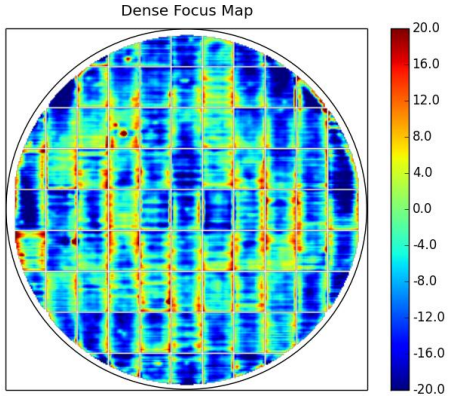
With subsequent SEM based verification and Scanner focus optimization

Simulated & through SMO optimized die based Process Window Map



X

Measured actual product wafer Defocus Map



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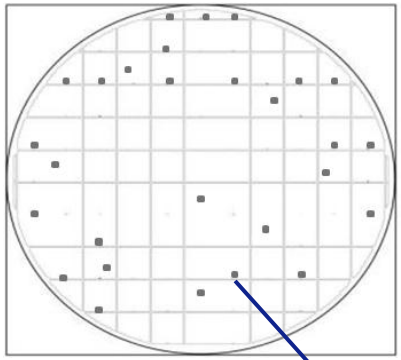
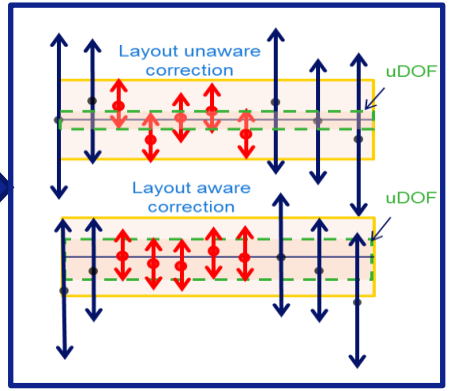
Patterning defect map prediction trough PW/DM maps convolution



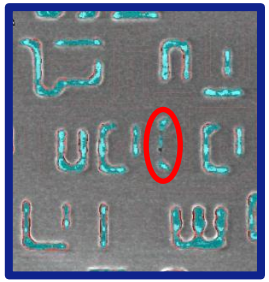
Defect Focus optimization using scanner knobs



Tachyon

Scanner & YieldStar Metrology

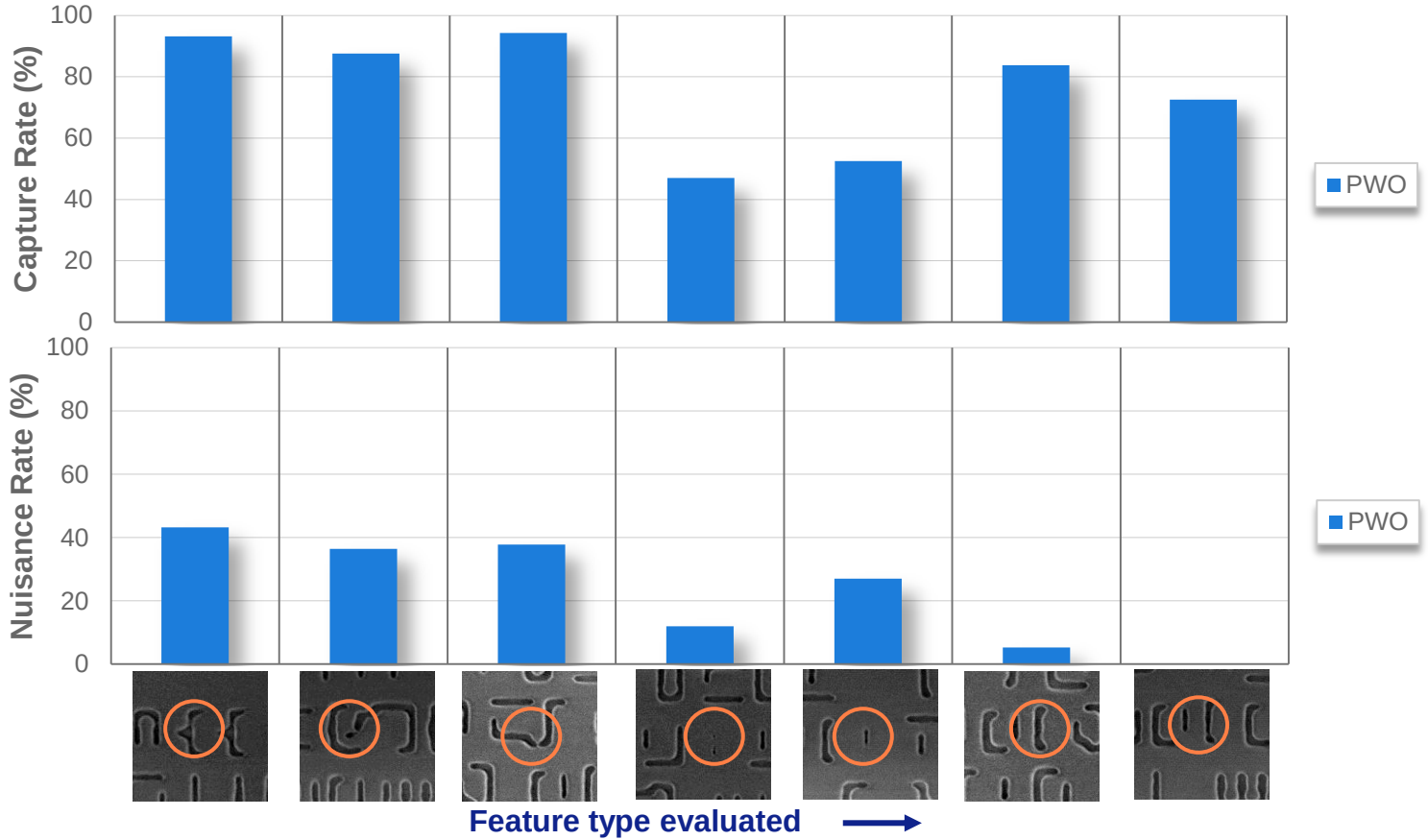
Defect prediction based followed by verification



Scanner

Good prospects Process Window Optimization

Capturing more defects vs. POR Inspection as verified by SEM



ASML holistic lithography: links the scanner to YieldStar metrology and computational lithography design context

Scanner performance with control knobs & interfaces to enable correction of errors outside of scanner

NXT - Immersion

NXE - EUV

1.Advanced lithography capability

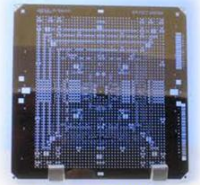
Modeling capability via computational lithography with unique design/scanner knowledge

4. Process Window Enlargement

Process control loops seamlessly integrated with scanner control capability to deliver ultimate on product performance

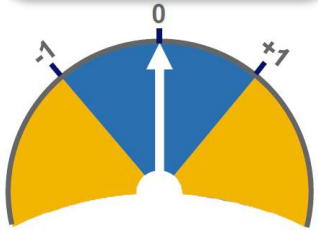
5. Process Window Control

Metrology provides accurate (design aware) volume data to enable correction capability

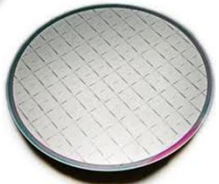


Product reticles

3- Computational Lithography Design context



6. Process window detection



Product wafers

2- YieldStar Metrology and Control SW

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